Remarks

Reconsideration of this Application is respectfully requested.

Claims 12-20 are pending in the application, with claim 12 being the independent claim. Claims 1-11 were previously cancelled.

Based on the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections Under 35 U.S.C. § 102(b)

The Examiner has rejected claims 12, 13, 16, 19 and 20 under 35 U.S.C. § 102(b) as being anticipated by Johnson, SUPERSCALAR MICROPROCESSOR DESIGN ("Johnson"). Based on the following remarks, Applicants respectfully traverse.

Claim 12 is directed to a system for renaming source registers of instructions stored in an instruction window of a processor, wherein the instruction window comprises a plurality of storage locations each of which stores a single instruction and wherein only a subset of the plurality of storage locations may be filled with new instructions in a single processor cycle. The claimed system includes:

> control logic that assigns one of a plurality of tags to a new instruction in the instruction window, each of said plurality of tags uniquely identifying a register for storing a result corresponding to an instruction in the instruction window;
>
> a data dependency checker that determines if said new instruction is dependent on another instruction in the instruction window by comparing a source register address of said new instruction with a destination register address of said other instruction in the instruction window; and

> tag assignment logic that outputs a renamed source register address for said new instruction, wherein said renamed source register address comprises a tag assigned to said other instruction in the instruction window if said new instruction is dependent on said other instruction.

Johnson does not teach or suggest each and every one of the foregoing features of claim 12. For example, Johnson does not teach or suggest "control logic that assigns one of a plurality of tags to a new instruction in the instruction window, *each of said plurality of tags uniquely identifying a register for storing a result corresponding to an instruction in the instruction window.*" The text in Johnson cited by the Examiner as teaching this feature relates to a register renaming scheme based on the use of a "reorder buffer". In accordance with this scheme:

> [w]hen an instruction is decoded, its result value is assigned a reorder-buffer location, and its destination-register number is associated with this location; this renames the destination register to the reorder-buffer location. A *tag,* or temporary hardware identifier, is created by hardware to identify the result, and the tag is also stored in the assigned reorder-buffer location. When a subsequent instruction refers to the re-named destination register, in order to obtain the value considered to be stored in the register, the instruction obtains instead the value stored in the reorder buffer or the tag for this value if the value has not yet been computed.

See Johnson at p. 48 (emphasis in original). Thus, in Johnson, a tag is used to "identify a result" and is stored in the assigned reorder-buffer location. The tag acts as a placeholder for the result value until such time as the result value has been computed.[1] The tag is not

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[1] As further explained at page 49 of Johnson:

> When an instruction is decoded, the register numbers of its source operands are used to access the reorder buffer and the register file at the same time. . . . If the reorder buffer does have a matching entry, the value in this entry is selected because this value must be the value most recently assigned to the register. If the value is not available, because it has not bee computed yet, the tag for the value is selected. In any case, the value or tag is copied to the reservation station.
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> * * *
>
> When a result is produced, it is written to the reorder buffer and to any reservation-station entry containing a tag for this result (this requires comparators in the reservation stations).

used, however, to "uniquely identify" a register in the reorder-buffer (i.e., the tag is not used as an address). Rather, in Johnson, each entry in the reorder-buffer is identified only by the register number that is written into it:

> [A]n entry in the reorder buffer is identified by specifying something that the entry *contains*, rather than by identifying the entry directly. In this case, the entry is identified using the register number that has been written into it. When a register number is presented to the reorder buffer, the reorder buffer provides the latest value written into the register (or a tag for the value if the value is not yet computed).

See Johnson at p. 49 (emphasis in original). In contrast, in claim 12, each of the recited plurality of tags uniquely identifies "a register for storing a result corresponding to an instruction in the instruction window." As explained in the specification of the present application with reference to an exemplary embodiment:

> The TAL [Tag Assignment Logic] determines the location in the temp buffer of the operands of dependent instructions. As noted above all instructions are assigned a tag that remains constant while the instruction is in the window, and there is one location in the temp buffer for each instruction in the window. ***Thus, the processor implementing the present invention uses the tag of an instruction as the temp buffer address of that instruction's result.***

Specification at paragraph [0041] (emphasis added).

Since Johnson does not teach or suggest each and every feature of independent claim 12, it cannot anticipate that claim. Accordingly, the Examiner's rejection of claim 12 under 35 U.S.C. § 102(b) is traversed and Applicants respectfully request that the rejection be reconsidered and withdrawn. Furthermore, claims 13, 16, 19 and 20 are also not anticipated by Johnson for at least the same reasons as claim 12 from which they depend and further in view of their own respective features. Accordingly, the Examiner's

rejection of claims 13, 16, 19 and 20 under 35 U.S.C. § 102(b) is traversed and Applicants respectfully requests that the rejection be withdrawn.

Judicially-Created Double Patenting Rejections

The Examiner has rejected claims 12-14 under the judicially created doctrine of double patenting over claim 7 of U.S. Patent No. 5,590,295, claims 7 and 14 of U.S. Patent No. 6,138,231, claims 8-11 of U.S. Patent No. 6,272,617 and claims 10-12 of U.S. Patent No. 6,408,375. The Examiner has also rejected claims 12, 17 and 18 under the judicially created doctrine of double patenting over claim 1 or 13 of U.S. Patent No. 5,809,276. Applicants have filed herewith a Terminal Disclaimer to Obviate a Double Patenting Rejection over each of U.S. Patent Nos. 5,590,295, 5,809,276, 6,138,231, 6,272,617 and 6,408,375, thereby rendering these rejections moot. Accordingly, Applicants respectfully request that the double patenting rejections of claims 12-14, 17 and 18 be reconsidered and withdrawn.

Claim Objections

The Examiner has objected to claim 15 as being dependent upon rejected claim 12. Based on the foregoing remarks, the rejection of claim 12 has been traversed. Therefore, Applicants respectfully request that the objection to claim 15 be reconsidered and withdrawn.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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